Due Date: 5/11/2016

To: SB Park, ME 517 Instructor

From: Tyler Wei

Subject: ANSYS FINAL

Problem Statement and Element Type/Model

Most computing devise now contain an internal BGA (Ball Grid Array) for microships into their circuit boards. When these devices are used, they will often overheat, thus strains are induced, and therefore deformations may occur internally. For this case study, the structure of a stacked die was analyzed from an internal heat generation with convection occurring at all sides. There are several materials involved in this model: printed circuit boards, silicon chips, and the underfills between the layers are examined in ANSYS to calculate the temperature distribution as well as the stresses that are induced thermally. As shown in Figure 1, the stacked die is composed of a PCB which is connected to the silicon chips by an array of solder balls. An underfill exists between the layers, surrounding the solder balls. This structure is then repeated again for a top layer with a series of small solder balls.

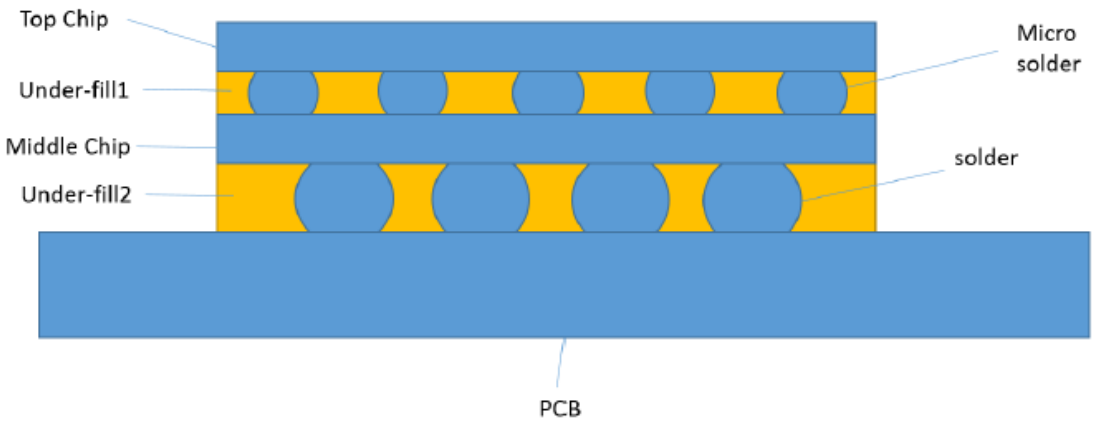

Figure 1. Problem sketch

The material properties of the various involved materials were provided as such in Table 1

Table 1. Material properties

	Young's Modulus(Gpa)	Poison's ratio	Coefficient of thermal expansion	Thermal conductivity (W/(m·K))
Chip	131	0.28	2.8e-6	130
Cu pad	110	0.34	16.4e-6	401
Solder	45.3	0.4	24e-6	50
PCB	31.75	0.28	16e-6	0.85
Underfill	8	0.4	35e-6	2

Model and Meshing

In order to optimize computational time and to minimize deviations in accuracy, idealizations as well as symmetry needed to be applied to the problem. Next, the given boundary conditions were applied to the model, simulating convection around the structure as well as some type of internal heat generation. Then, a solution was obtained from undergoing a thermal analysis to determine the temperature distribution throughout the stacked die. Finally, the stresses were plotted to figure out the stresses within the model resulting from thermal expansion.

As mentioned, efficient modelling practices is crucial in optimizing script running time. A quarter symmetry was utilized due to the geometric properties. Initially, the micro solders were rendered because it appears at the model origin, followed by the generation of the solders. Every individual solder needed to be assembled through every layer of the die to properly mesh as shown in Figure 2. Both the silicon chips, the PCB, as well as the underfills were then generated and modelled through the use of the BLC4 command. There are global interferences with the volumes of the components and they are trimmed off at a later step.

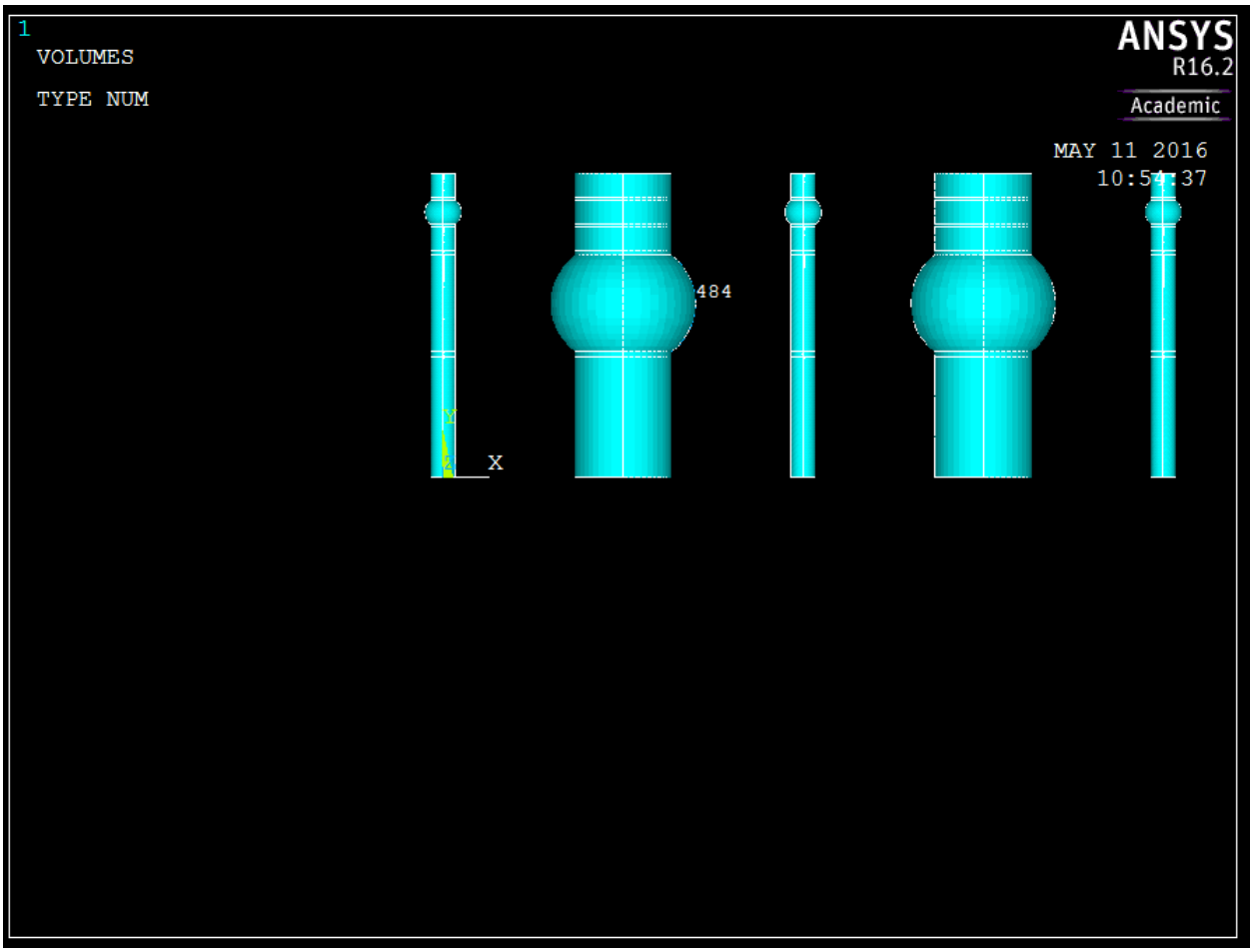

Figure 2. Solder models

Material properties then needed to be assigned and several of the lines were resized in order to ensure proper meshing geometries. The aforementioned volumetric global interferences were then deleted from the models to produce a clean cut through the middle of the die. The commands utilized for the model to size and mesh are the VOVLAP and the VGLUE commands. The remaining material properties and linear geometries were then sized. As shown in the Figure 3, the model was finalized and ready to be

meshed. Below Figure 3 is Figure 4 and Figure 5, which delineates the model mesh. After the meshing, the applications of the boundary conditions will lead to the analytical solution.

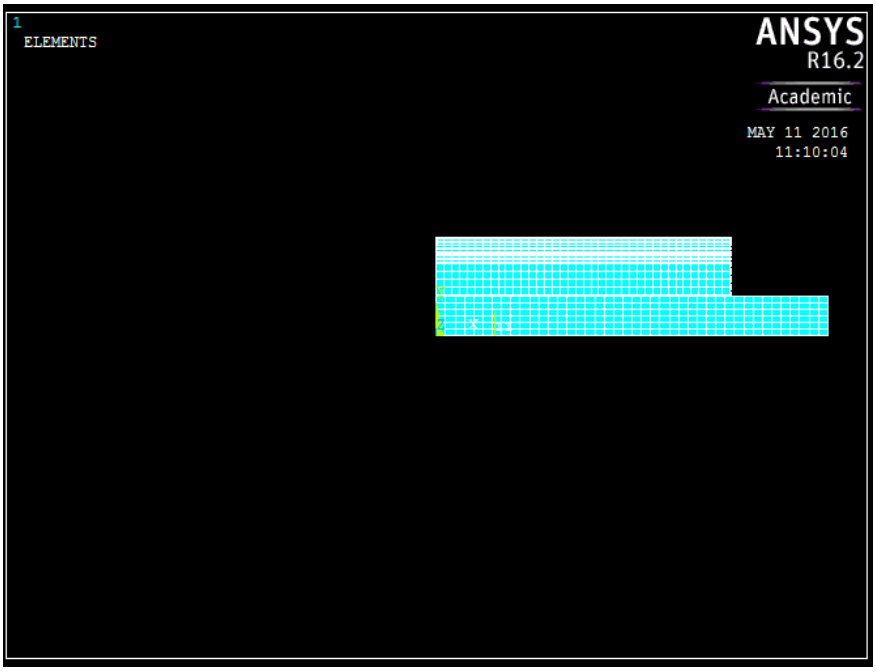

Figure 3. Meshing (A)

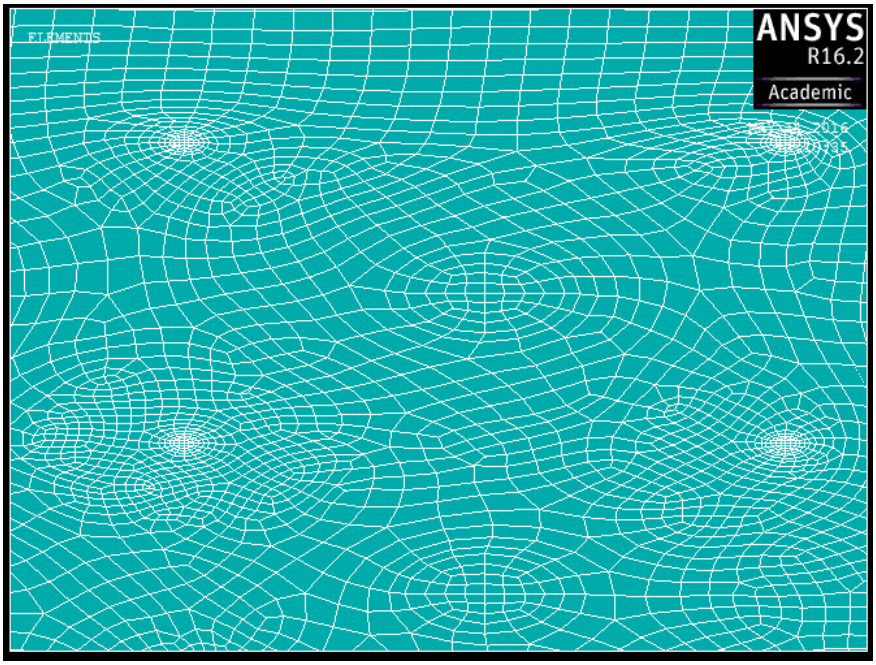

Figure 4. Meshing (B)

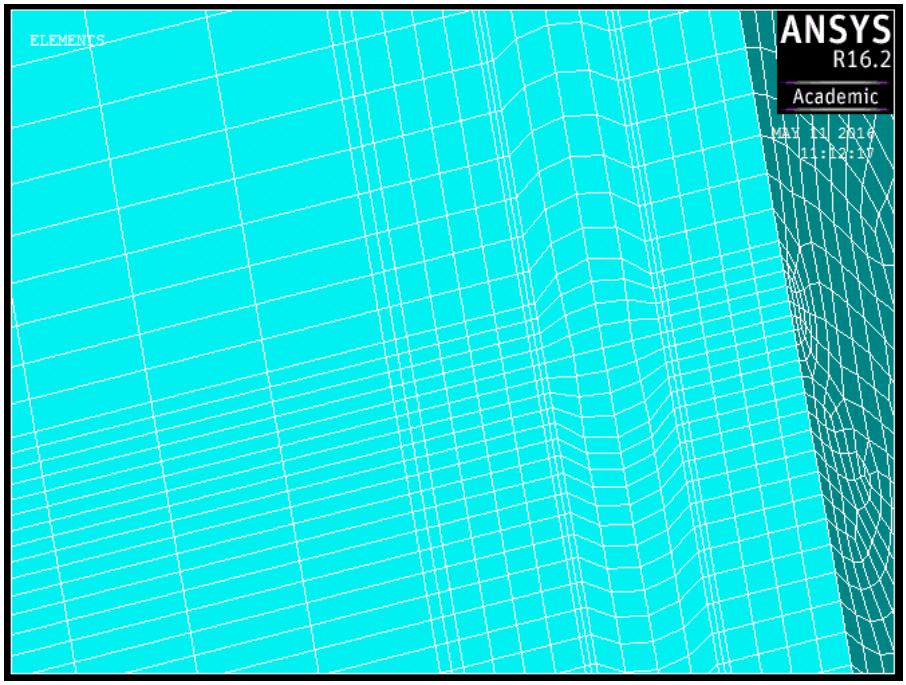

Figure 5. Meshing (C)

Boundary Conditions

Thermal Analysis

As mentioned before the boundary conditions were provided as there is an internal heat generation as well as convection occurring at all surfaces of the stacked die. First a thermal analysis was initiated to the model. The convection constraints were first taken into account. All of the externally placed nodes were selected via the NSEL,EXT command, next all the nodes on the model-cut surfaces were deselected. After unit conversion, the offset temperature was determined to be 273 degrees Celsius. Next, the boundary conditions for convection were applied. This involves the inclusion of the coefficient of convective heat transfer as well as the ambient temperature which was set to 25 degrees Celsius. The conditions of internal heat generation was then applied to the middle chip. The initial uniformly distributed temperature (25 degrees Celsius) was then simulated throughout the entire structure of the die. As shown in Figure 6, the boundary conditions are marked and indicated. Below that, Figure 7 shows the fringe plot of the temperature distribution.

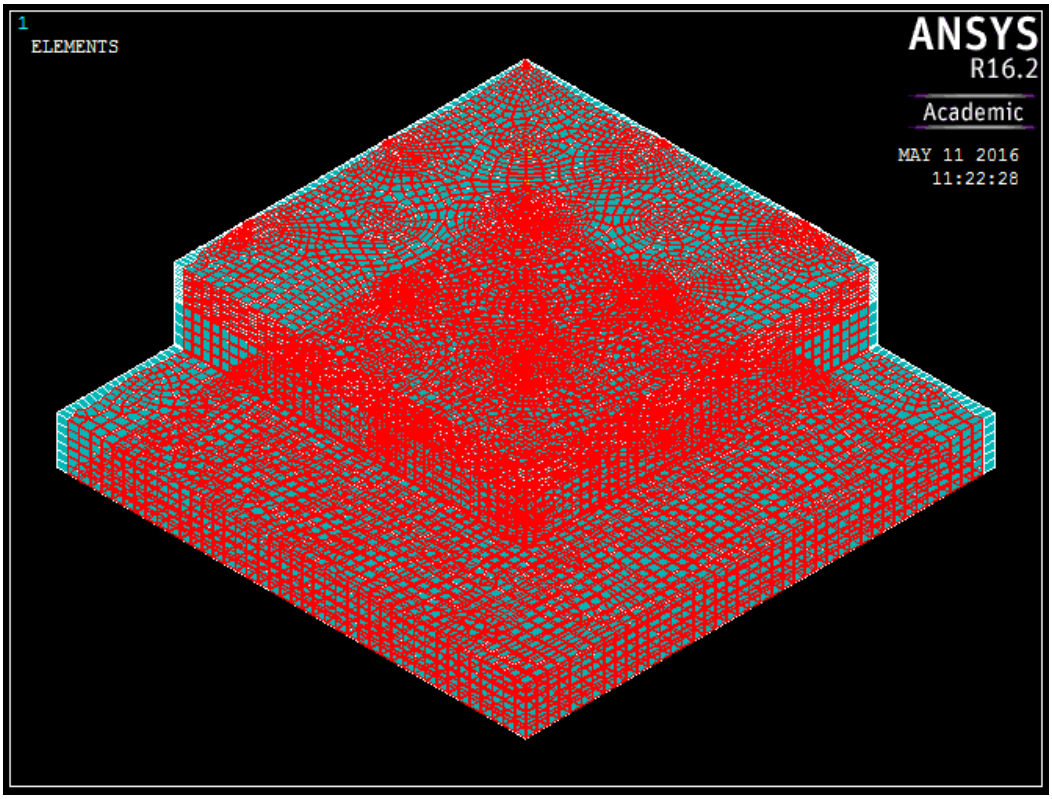

Figure 6.Thermal Boundary Conditions

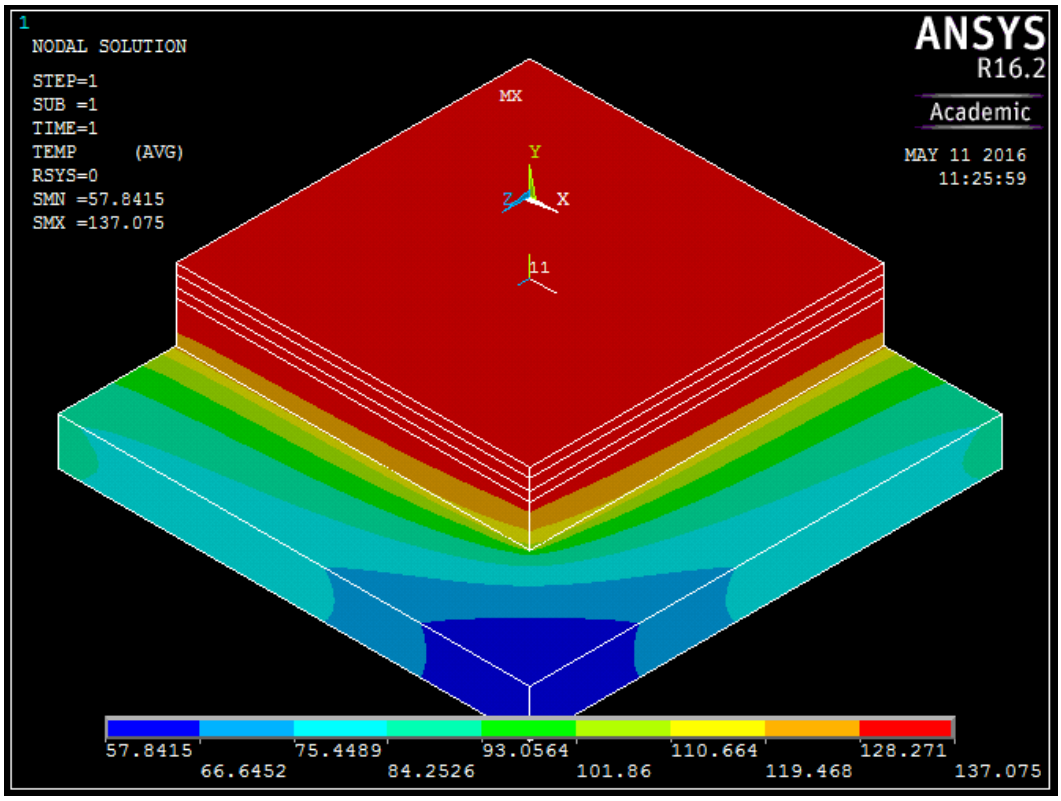

Figure 7. Thermal Fringe Plot

Structural Analysis

In order to take into account the additional degrees of freedom, the model had its element type changed from SOLID70 to a SOLID85. The surface cut nodes were then constrained from moving in the X and Z directional displacements. The node at the origin was then constrained in the Y directional displacement. The temperature distribution was then applied from the thermal analysis and then the SOLVE command was utilized. Figure 8, displays the fringe plot of the stresses. From analysis of previous situations regarding the BGA, the maximum stresses will typically occur at the connections at the copper pads which link together the solder balls to the chips/PCB. As a result of this phenomena, Figure 8 delineates the magnitude as well as location of the maximum stresses within the copper pads. The displacements at the individual points adjacent to the line from the origin to the corner are shown on this plot.

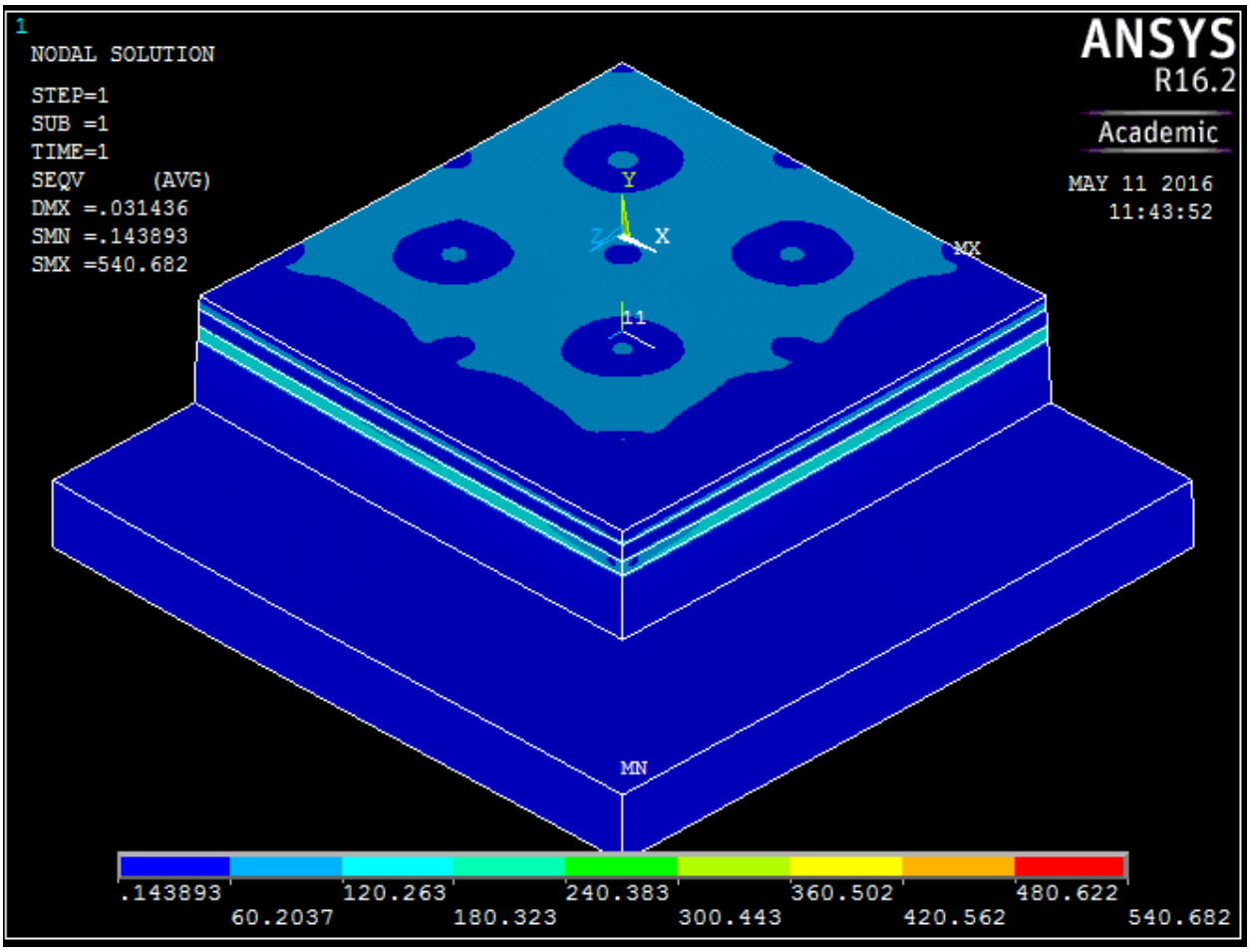

Figure 8. Stress Fringe Plot

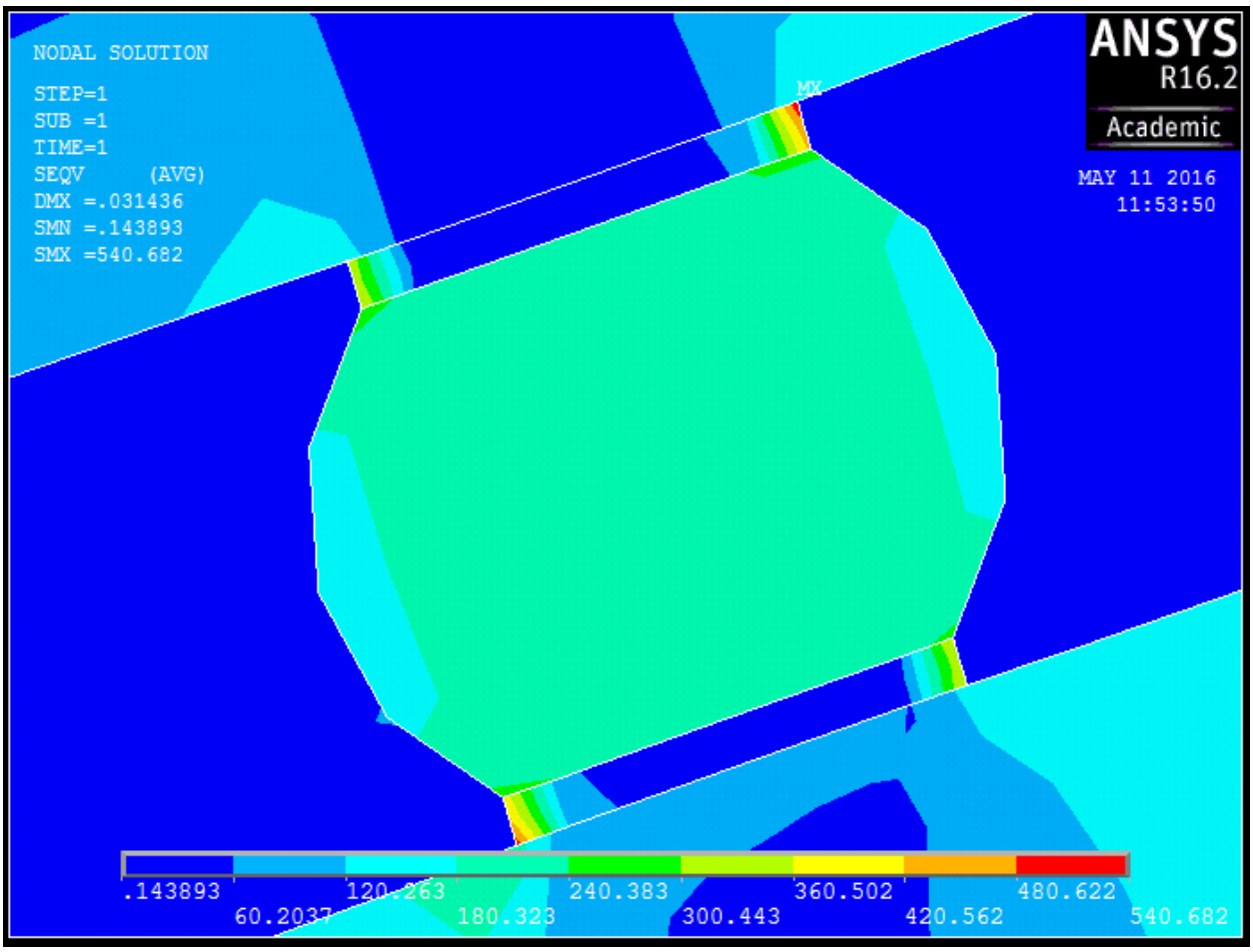

Figure 9. Maximum Stress at Copper Pads

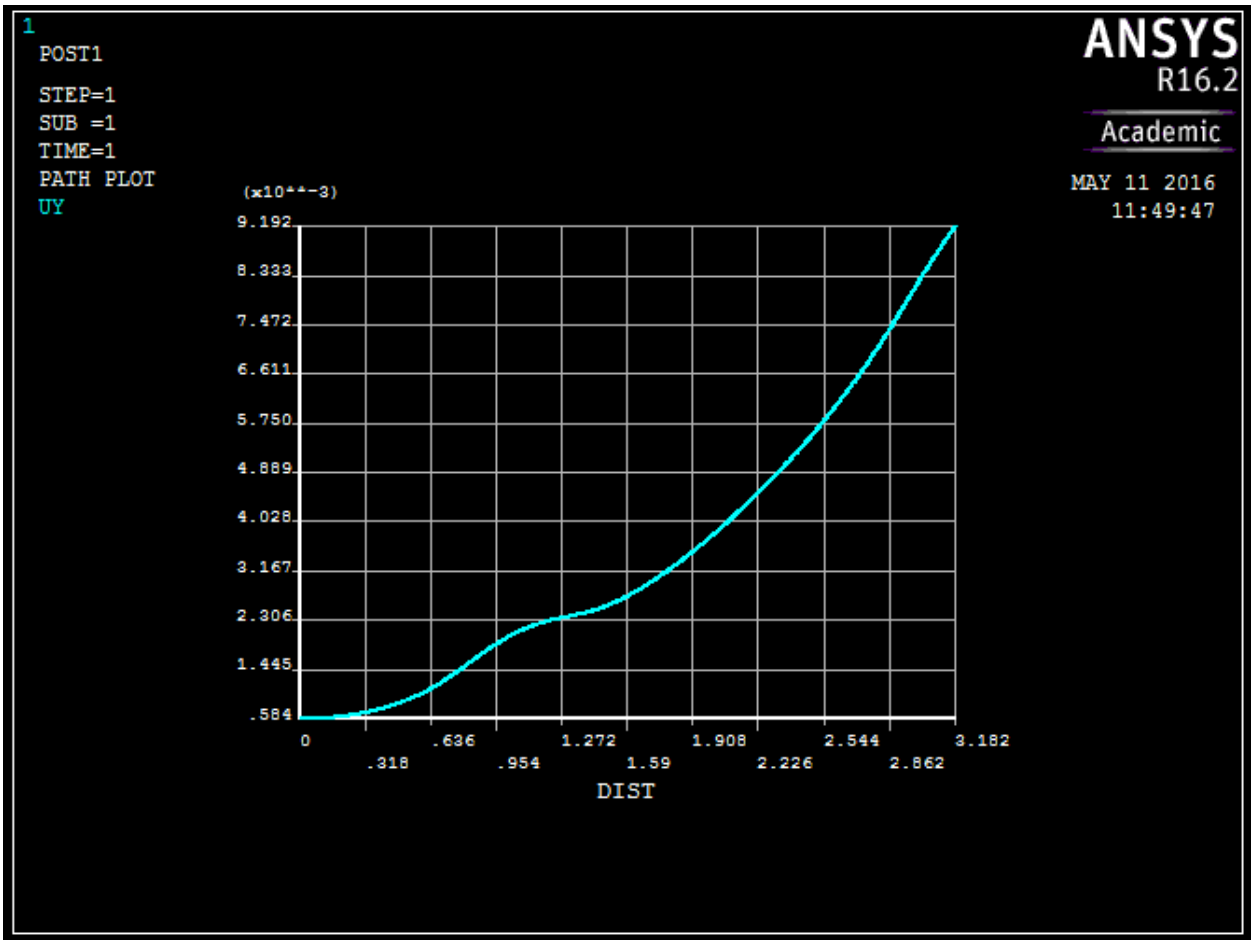

Figure 10. Displacement Plot

Results and Discussion

From the ANSYS APDL thermodynamic computational analysis, the maximum temperature in the stacked BGA die was determined to be 137 degrees Celsius. The structural analysis determined the maximum stress of 540 MPA to exist in the copper pads, as expected from the results of the 2 dimensional as well as the 3 dimensional BGA problems previously examined. The maximum displacement was 3.168 mm.

ANSYS ADPL Code

```
finish
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/filename,Wei_Tyler_ME_517_ANSYS_Final
/prep7
et,1,solid70
!Chip
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MP,NUXY,1,0.28
MP,ALPX,1,2.8e-6
MP,KXX,1,130e-3
!Cu Pad
MP,EX,2,110e3
MP,NUXY,2,0.34
MP,ALPX,2,16.4e-6
MP,KXX,2,401e-3
!Solder
MP,EX,3,45.3e3
MP,NUXY,3,0.4
MP,ALPX,3,24e-6
MP,KXX,3,50e-3
!PCB
MP,EX,4,31.75e3
MP,NUXY,4,0.28
MP,ALPX,4,16e-6
MP,KXX,4,0.85e-3
!Underfill
MP,EX,5,8e3
MP,NUXY,5,0.4
MP,ALPX,5,35e-6
MP,KXX,5,2e-3
!Micro Solder
blc4,0,0,0.05,0.5
blc4,0,0.5,0.05,0.02
blc4,0,0.52,0.05,0.4
blc4,0,0.92,0.05,0.02
blc4,0,0.94,0.05,0.1
blc4,0,1.04,0.05,0.01
blc4,0,1.15,0.05,0.01
blc4,0,1.16,0.05,0.1
l,24,25
k,,0.075,1.1
larc,23,26,33
al,23,33,25,34
aglue,all
numcmp,all
vrotat,all,,,,,,1,20,90
alls
vsymm,x,all
alls
vsymm,z,all
nummrg,all
alls
vgen,3,all,,,1.5
alls
vgen,3,all,,,,,1.5
!Solder
local,11,0,0.75,,0.75
csys,11
wpcsys,,11
blc4,0,0,0.2,0.5
blc4,0,0.5,0.2,0.02
blc4,0,0.92,0.2,0.02
blc4,0,0.94,0.2,0.1
blc4,0,1.04,0.2,0.01
blc4,0,1.05,0.2,0.1
blc4,0,1.15,0.2,0.01
blc4,0,1.16,0.2,0.1
numcmp,all
l,459,460
k,,0.3,0.72
larc,458,461,484
al,1158,1134,1159,1132
numcmp,all
asel,s,loc,x,0,0.3
vrotat,all,,,,,,452,483,90
vsel,s,loc,x,0,0.3
vsymm,x,all,,,0,0
vsymm,z,all,,,0,0
vgen,2,all,,,1.5
vgen,2,all,,,,,1.5
!Matl Prop
alls
csys,0
wpcsys,,1
vsel,s,loc,y,1.05,1.15
vsel,u,loc,x,0.25,1.05
vsel,u,loc,x,1.95,2.55
vatt,3
vsel,s,loc,y,0.52,0.92
vsel,u,loc,x,-1,0.3
vsel,u,loc,x,1.06,1.94
vsel,u,loc,x,2.56,5
vatt,3
vsel,s,loc,y,0.5,0.52
vsel,a,loc,y,0.92,0.94
vsel,a,loc,y,1.04,1.05
vsel,a,loc,y,1.15,1.16
vatt,2
alls
!Meshing
lsel,s,loc,y,0.941,1.039
lsel,a,loc,y,1.051,1.149
lsel,a,loc,y,1.161,1.259
lesize,all,,,4
lsel,s,loc,y,0
lsel,a,loc,y,0.5
lsel,a,loc,y,0.52
lsel,a,loc,y,0.92
lsel,a,loc,y,0.94
lsel,a,loc,y,1.04
lsel,a,loc,y,1.05
lsel,a,loc,y,1.15
lsel,a,loc,y,1.16
lsel,a,loc,y,1.26
lsel,u,length,,0.01
lesize,all,,,4
alls
!Chip layer
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blc4,0,1.16,3.75,0.1,3.75
!underfills
blc4,0,0.5,3.75,0.02,3.75
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blc4,0,0.92,3.75,0.02,3.75
blc4,0,1.04,3.75,0.01,3.75
blc4,0,1.15,3.75,0.01,3.75
blc4,0,1.05,3.75,0.1,3.75
!PCB
blc4,0,0,3.75,0.5,3.75
blc4,0,0,5,0.5,5
!touchup
vsel,s,loc,x,-1,0
vsel,a,loc,z,-1,0
vdele,all,,,1
alls
nummrg,all
vovlap,all
vglue,all
numcmp,all
!Matl prop
vsel,s,loc,y,0,0.5
vatt,4
vsel,s,loc,y,0.5,0.52
vsel,a,loc,y,0.92,0.94
vsel,a,loc,y,1.04,1.05
vsel,a,loc,y,1.15,1.16
vsel,a,loc,y,0.52,0.92
vsel,a,loc,y,1.05,1.15
vsel,u,mat,,2
vsel,u,mat,,3
vatt,5
vsel,s,loc,y,1.16,1.26
vsel,a,loc,y,0.94,1.04
vatt,1
!complete meshing
alls
lsel,s,length,,0.01
lesize,all,,,2
lsel,s,length,,0.02
lesize,all,,,2
lsel,s,length,,3.75
lesize,all,,,38
lsel,s,length,,1.4
lesize,all,,,28,-3
lsel,s,length,,0.7
lesize,all,,,24,4
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lesize,all,,,6
lsel,s,length,,0.4
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lesize,all,,,18
lsel,s,length,,5
lesize,all,,,42
lsel,s,length,,0.1
lesize,all,,,4
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lesize,all,,,4
alls
vsweep,all
!Solution Thermo
/solu
antype,static
alls
toffst,273
tunif,25
nsel,s,ext
nsel,u,loc,x,0
nsel,u,loc,z,0
sf,all,conv,100e-6,25
vsel,s,loc,y,0.941,1.039
bfv,all,hgen,0.5/(3.75*3.75*0.1)
alls
solve
finish
!Post Processing
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plnsol,temp
!Solution Structural
/prep7
et,1,solid185
!Chip
MP,EX,1,131e3
MP,NUXY,1,0.28
MP,ALPX,1,2.8e-6
MP,KXX,1,130e-3
!Cu Pad
MP,EX,2,110e3
MP,NUXY,2,0.34
MP,ALPX,2,4.8e-6
MP,KXX,2,401e-3
!Solder
MP,EX,3,45.3e3
MP,NUXY,3,0.4
MP,ALPX,3,24e-6
MP,KXX,3,50e-3
!PCB
MP,EX,4,31.75e3
MP,NUXY,4,0.28
MP,ALPX,4,16e-6
MP,KXX,4,0.85e-3
!Underfill
MP,EX,5,8e3
MP,NUXY,5,0.4
MP,ALPX,5,35e-6
MP,KXX,5,2e-3
!Structural BC
/solu
nsel,s,loc,x,0
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d,all,uz,0
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d,all,uy,0
alls
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ldread,temp,,,,,,rth
solve
finish
!Post Processing
/post1
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PLPATH,UY
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